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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/285,899	04/08/1999	SHUNPEI YAMAZAKI	0756-1950	4276

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EXAMINER	
DUDEK, JAMES A	
ART UNIT	PAPER NUMBER
2871	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/285,899	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	/James A. Dudek/	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-16,21-24,33-36,50-52,54 and 57-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-16,21-24,33-36,50-52,54 and 57-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 07/857,597.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/7/05,10/8/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-16, 21-24, 33-36, 50-52, 54 and 57-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba (US 5227900) in view of Takeshita (JP 61-141174) and Wakai et al (US 5055899).

Inaba discloses all except for a leveling (organic resin) layer on the TFT and the pixel electrode on the leveling layer. See other detailed explanations in the office action mailed 06-05-01, if needed.

Takeshita teaches that the use of leveling film of organic resin over the TFT for an active matrix substrate is common (an usual way) in the art. Wakai discloses (see Figures 1-2) that a conventional active matrix substrate comprising a thin film transistor having a pixel electrode directly connected to the drain electrode suffers several disadvantages such as short-circuiting, thus, it is hard to obtain a TFT which can stably operate without causing a short-circuiting between the pixel electrode and the drain electrode (see col. 2, lines 18-27, lines 63-68; Inaba discloses this similar conventional structure of having the pixel electrode directly connected to the drain electrode). Wakai solves the short-circuiting problem by forming the insulation/leveling layer (e.g., organic resin) between the pixel electrode and the drain electrode, wherein the pixel electrode is electrically connected to the drain electrode through a contact hole of the insulation layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an insulating/leveling layer having a contact hole and formed between the pixel electrode and the drain electrode for avoiding disadvantages including short-circuiting, i.e., a leveling (organic resin) layer on the TFT and the pixel electrode on the leveling layer, as taught by Takeshita and Wakai.

(10) Response to Argument

Applicant's arguments are as follows:

(A) Request for consideration of Information Disclosure Statements.

(B) The present claims are not prima facie obvious based on the combination of Inaba (US 5227900) in view of Takeshita (JP 61-141174) and Wakai (US 5055899), i.e., the Office Action has not established a prima facie case of obviousness (three basis criteria steps have not been met) based on the following arguments:

(B1) Inaba fails to disclose the pixel electrode electrically connected to the TFT/semiconductor element through an opening formed in the organic resin/leveling film.

(B2) Takeshita (the secondary reference) appears to teach the TFT substrate for the solid state image pickup device, and thus the device in Takeshita would not able to incorporate in the device of Inaba, (the main reference, the display device being a liquid crystal display device and also employing ferroelectric liquid crystal material).

(B3) Takeshista fails to provide a proper motivation.

(B4) Inaba (published in 1993) was aware to the teachings of Takeshita (published in 1986). If it were important to have leveling layer in a liquid crystal display device, particularly one formed between a TFT and pixel electrode, then why is Inaba as silent as to the importance of such feature? Thus, it was not obvious at the time of the invention that it would have been desirable to provide a liquid crystal panel with a leveling layer formed between a TFT and a pixel electrode of the liquid crystal panel.

(B5) Wakai fails to disclose the leveling layer, rather discloses an insulating layer.

(B6) Inaba (the main reference) does not seem to be concerned with the short-circuiting problem that device of Wakai (the secondary reference). Thus, there is no reason to combine Wakai to the device of Inaba.

Examiner's responses to Applicant's arguments are as follows:

(A) Initialed IDS copies are enclosed.

(B1) The rejection is under 35 USC 103, not 35 USC 102. Inaba, the main reference, discloses the claimed invention except for the pixel electrode electrically connected to the TFT/semiconductor element through an opening formed in the organic resin/leveling film, as noted in the office action. The office action relies on the secondary references (Takeshita and Wakai) to teach this limitation that lacks from Inaba. Takeshita teaches that the use of leveling film of organic resin over the TFT is common (an usual way) in the art. Further, Wakai discloses (see figures 1-2) that an active matrix substrate comprising a thin film transistor having a pixel electrode directly connected to the drain electrode suffers several disadvantages such as short-circuiting, thus, it is hard to obtain a TFT which can stably operate without causing a short-circuiting between the pixel electrode and the drain electrode (see col. 2, lines 18-27, lines 63-68; Inaba discloses this similar conventional structure of having the pixel electrode directly connected to the drain electrode). Wakai solves the short-circuiting problem by forming the insulation layer (e.g., organic resin) between the pixel electrode and the drain electrode, wherein the pixel electrode is electrically connected to the drain electrode through a contact hole of the insulation layer.

(B2) Takeshita discloses an active matrix substrate comprising a transparent substrate, a TFT formed on the transparent substrate including elements such as gate electrode, gate insulator, channel region, source and drain electrodes, an insulator formed on the TFT, a pixel electrode formed on the insulator. This is a common active matrix substrate for a liquid crystal display device (see at least Wakai, Figure 3). TFTs are merely used as driving switching-elements that individually drive pixel electrodes in any liquid crystal display device including twisted nematic LCD device, ferroelectric LCD device.

(B3) Takeshita teaches that the use of leveling film of organic resin over the TFT is common (an usual way) in the art. Further, Wakai discloses (see figures 1-2) that an active matrix substrate comprising a thin film transistor having a pixel electrode directly connected to the drain electrode suffers several disadvantages such as short-circuiting, thus, it is hard to obtain a TFT which can stably operate without causing a short-circuiting between the pixel electrode and the drain electrode (see col. 2, lines 18-27, lines 63-68; Inaba discloses this similar conventional structure of having the pixel electrode directly connected to the drain electrode). Wakai solves the short-circuiting problem by forming the insulation layer (e.g., organic resin)

between the pixel electrode and the drain electrode, wherein the pixel electrode is electrically connected to the drain electrode through a contact hole of the insulation layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an insulating layer (organic resin) having a contact hole and formed between the pixel electrode and the drain electrode for avoiding disadvantages including short-circuiting, i.e., a leveling (organic resin) layer on the TFT and the pixel electrode on the leveling layer.

(B4) The comparison between the main reference's date and the secondary reference's date is irrelevant under 35 USC 103. The main and secondary references each provides a date that is prior to the effective filing date of the application, thus constitutes as prior art. The main reference(Inaba) discloses the claimed invention except for the pixel electrode electrically connected to the TFT/semiconductor element through an opening formed in the organic resin/leveling film, as noted in the office action. The office action relies on the secondary references (Takeshita and Wakai) to teach this limitation that lacks from Inaba.

(B5) Wakai discloses the insulating film 108 filling recesses generated upon formation of the above thin films and *flatten* (level) the surface above the insulating substrate (see at least col. 4, lines 52-54).

(B6) In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Takeshita teaches that the use of leveling film of organic resin over the TFT for an active matrix substrate is common (an usual way) in the art. Wakai discloses (see Figures 1-2) that a conventional active matrix substrate comprising a thin film transistor having a pixel electrode directly connected to the drain electrode suffers several disadvantages such as short-circuiting, thus, it is hard to obtain a TFT which can stably operate without causing a short-circuiting between the pixel electrode and the drain electrode (see col. 2, lines 18-27, lines 63-68; Inaba discloses this similar conventional structure of having the pixel electrode directly

connected to the drain electrode). Wakai solves the short-circuiting problem by forming the insulation/leveling layer (e.g., organic resin) between the pixel electrode and the drain electrode, wherein the pixel electrode is electrically connected to the drain electrode through a contact hole of the insulation layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an insulating/leveling layer having a contact hole and formed between the pixel electrode and the drain electrode for avoiding disadvantages including short-circuiting, i.e., a leveling (organic resin) layer on the TFT and the pixel electrode on the leveling layer, as taught by Takeshita and Wakai.

The office action has been established a prima facie case of obviousness (three basis criteria steps have been met), as explained above, and thus the present claims are prima facie obvious based on the combination of Inaba (US 5227900) in view of Takeshita (JP 61-141174) and Wakai (US 5055899).

Conclusion

This is a Request for Continued Examination. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to /James A. Dudek/ whose telephone number is 571-272-2290. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/James A. Dudek/
Primary Examiner
Art Unit 2871